CLAIMS

What is claimed is:

1. A processor comprising:

a first processing entity;

a second processing entity; and

a plurality of registers to allow communication between the first processing entity and the second processing entity, wherein the plurality of registers are cross-decoded by the first processing entity and the second processing entity.

2. A processor as recited in claim 1, wherein the first and second processing entities are separate cores of the processor.

3. A processor as recited in claim 1, wherein the first and second processing entities are separate threads of the processor.

4. A microprocessor comprising:

a first core;

a second core;

a first register to communicate information from the first core to the second core, wherein the first register is decoded by the first core to have a first register name and is decoded by the second core to have a second register name; and

a second register to communicate information from the second core to the first core, wherein the second register is decoded by the first core to have the second register name and decoded by the second core to have the first register name.

5. A microprocessor as recited in claim 4, wherein the first register is to communicate information only from the first core to the second core, and the second register is to communicate information only from the second core to the first core.

6. A microprocessor as recited in claim 4, wherein the first and second registers each include a bit used to synchronize operation of the first core and the second core.

7. A multi-thread microprocessor comprising:

a core to execute a first thread concurrently with a second thread;

a first register to communicate information from the first thread to the second thread, wherein the first register is decoded by the first thread to have a first register name and is decoded by the second thread to have a second register name; and

a second register to communicate information from the second thread to the first thread, wherein the second register is decoded by the first thread to have the second register name and decoded by the second thread to have the first register name.

8. A microprocessor as recited in claim 7, wherein the first register is to communicate information only from the first thread to the second thread, and the second register is to communicate information only from the second thread to the first thread.

9. A microprocessor as recited in claim 7, wherein the first and second registers each include a bit used to synchronize operation of the first thread and the second thread.

10. A microprocessor comprising:

a first processing entity;

a second processing entity;

a first register;

a second register;

means for using the first register to communicate information from the first processing entity to the second processing entity;

means for using the second register to communicate information from the second processing entity to the first processing entity; and

means for cross-decoding the first register and the second register between the first processing entity and the second processing entity.

11. A microprocessor as recited in claim 10, wherein the first and second processing entities are separate cores of the microprocessor.

12. A microprocessor as recited in claim 10, wherein the first and second processing entities are separate threads of the microprocessor.

13. A computer system comprising:

a microprocessor, the microprocessor including

a first core,

a second core,

a first register to communicate information only from the first core to the second core, wherein the first register is decoded by the first core to have a first register name and is decoded by the second core to have a second register name,

a second register to communicate information only from the second core to the first core, wherein the second register is decoded by the first core to have the second register name and decoded by the second core to have the first register name, and

a shared cache coupled to the first core and the second core;

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

14. A computer system as recited in claim 13, wherein the first register is to communicate information only from the first thread to the second thread, and the second register is to communicate information only from the second thread to the first thread.

15. A computer system as recited in claim 13, wherein the first and second registers each include a bit used to synchronize operation of the first core and the second core.

16. A multi-core microprocessor comprising:

a first core to operate based on a firmware layer;

a second core to operate based on the firmware layer; and

a hardware-based communication mechanism to allow communication between the first core and the second core, such that the first core and the second core can execute identical code paths of the firmware layer to communicate with each other.

17. A computer system as recited in claim 16, wherein the hardware-based communication mechanism comprises:

a first register to communicate information from the first core to the second core, wherein the first register is decoded by the first core to have a first register name and is decoded by the second core to have a second register name; and

a second register to communicate information from the second core to the first core, wherein the second register is decoded by the first core to have the second register name and decoded by the second core to have the first register name.

18. A computer system as recited in claim 17, wherein the first register is to communicate information only from the first core to the second core, and the second register is to communicate information only from the second core to the first core.

19. A computer system as recited in claim 18, wherein the first and second registers each include a bit used to synchronize operation of the first core and the second core.

20. A processor comprising:

a plurality of processing entities, each of the processing entities having associated therewith a first register to enable the processing entity to receive information relating to another processing entity of the plurality of processing entities and a second register to enable the processing entity to output information for use by another processing entity of the plurality of processing entities; and

a logic circuit to apply a logic operation to contents of the second register of each of the processing entities and to store a result of the logic operation in the first register of each of the processing entities.

21. A processor as recited in claim 20, wherein each of the plurality of processing entities is a separate core of the processor.

22. A processor as recited in claim 20, wherein each of the plurality of processing entities is a separate thread of the processor.

23. A multi-core microprocessor comprising:

a plurality of cores, each of the cores having associated therewith a first register to enable the core to receive information relating to another core of the microprocessor and a second register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the second register of each of the cores and to store a result of the logic operation in the first register of each of the cores.

24. A microprocessor as recited in claim 23, wherein the first register of each of the cores is a read-only register, and the second register of each of the cores is a read-write register.

25. A microprocessor as recited in claim 23, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

26. A microprocessor as recited in claim 23, wherein the logic circuit is programmable to select the logic operation.

27. A microprocessor as recited in claim 26, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

28. A multi-thread microprocessor comprising:

a core to execute a first thread concurrently with a second thread; and

a plurality of registers, including a first register for each of the threads to enable the thread to receive information relating to another thread of the microprocessor and a

second register for each of the threads to enable the thread to output information for use by another thread of the microprocessor; and

a logic circuit to apply a logic operation to contents of the second register of each of the threads and to store a result of the logic operation in the first register of each of the threads.

29. A microprocessor as recited in claim 28, wherein the first register of each of the threads is a read-only register, and the second register of each of the threads is a read-write register.

30. A microprocessor as recited in claim 28, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the threads.

31. A microprocessor as recited in claim 28, wherein the logic circuit is programmable to select the logic operation.

32. A microprocessor as recited in claim 31, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

33. A multi-core microprocessor comprising:

a plurality of cores, each of the cores having associated therewith

a read-only register to enable the core to receive information relating to another core of the microprocessor, and

a read-write register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the read-write register of each of the cores and to store a result of the logic operation in the read-only register of each of the cores.

34. A microprocessor as recited in claim 33, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

35. A microprocessor as recited in claim 33, wherein the logic circuit is programmable to select the logic operation.

36. A microprocessor as recited in claim 35, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

37. An apparatus comprising:

a first register for each of a plurality of processing entities of a microprocessor, to enable the processing entity to input information from outside the processing entity;

a second register for each of the processing entities, to enable the processing entity to output information;

means for applying a logic operation to contents of the second register of each of the processing entities; and

means for storing a result of the logic operation in the first register of each of the processing entities.

38. An apparatus as recited in claim 37, wherein each of the plurality of processing entities is a separate core of the microprocessor.

39. An apparatus as recited in claim 37, wherein each of the plurality of processing entities is a separate thread of the microprocessor.

40. An apparatus as recited in claim 37, wherein said means for applying a logic operation comprises means for applying the logic operation in a bit-wise manner.

41. A computer system comprising:

a microprocessor including a plurality of cores, each of the cores having associated therewith

a read-only register to enable the core to receive information relating to another core of the microprocessor, and

a read-write register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the read-write register of each of the cores and to store a result of the logic operation in the read-only register of each of the cores, and

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

42. A computer system as recited in claim 41, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

43. A computer system as recited in claim 41, wherein the logic circuit is programmable to select the logic operation.

44. A computer system as recited in claim 43, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

45. A multi-core processor comprising:

a first core;

a second core; and

a register which includes a bit used to synchronize operation of the first core and the second core.

46. A processor as recited in claim 45, further comprising:

a second register which includes a bit used to synchronize operation of the first core and the second core;

wherein the first core is configured to execute a predetermined synchronization instruction by setting the bit in the first register to a predetermined value and then waiting until the bit in the second register is set to a predetermined value before proceeding.

47. A processor as recited in claim 46, wherein the second core is configured to execute the predetermined synchronization instruction by setting the bit in the second register to a predetermined value and then waiting until the bit in the first register is set to a predetermined value before proceeding.

48. A processor as recited in claim 47, wherein the first register and the second register are cross-decoded by the first core and the second core.

49. A multi-thread processor comprising:

a core to execute a first thread concurrently with a second thread; and

a register which includes a bit used to synchronize execution of the first thread and the second thread.

50. A processor as recited in claim 49, further comprising:

a second register which includes a bit used to synchronize operation of the first thread and the second thread;

wherein the first thread sets the bit in the first register to a predetermined value and then waits until the bit in the second register is set to a predetermined value before proceeding.

51. A processor as recited in claim 49, wherein the second thread sets the bit in the second register to a predetermined value and then waits until the bit in the first register is set to a predetermined value before proceeding.

52. A processor as recited in claim 51, wherein the first register and the second register are cross-decoded by the first thread and the second thread.

53. A multi-core microprocessor comprising:

a first core;

a second core; and

a first register shared by the first core and the second core to allow communication of messages between the first core and the second core, the first register including a bit used as a signal to synchronize operation of the first core and the second core.

54. A microprocessor as recited in claim 53, further comprising a second register shared by the first core and the second core to allow communication of messages between the

first core and the second core, the second register including a bit used as a signal to synchronize operation of the first core and the second core.

55. A microprocessor as recited in claim 54, wherein the first register and the second register are cross-decoded by the first core and the second core.

56. A microprocessor as recited in claim 55, wherein the first core is configured to execute a predetermined synchronization instruction by setting the bit in the first register to a predetermined value and then waiting until the bit in the second register is set to a predetermined value before proceeding.

57. A microprocessor as recited in claim 56, wherein the second core is configured to execute the predetermined synchronization instruction by setting the bit in the second register to a predetermined value and then waiting until the bit in the first register is set to a predetermined value before proceeding.

58. A microprocessor comprising:

a first core;

a second core;

a first register to communicate information from the first core to the second core, wherein the first register includes a plurality of bits used to synchronize operation of the first core and the second core; and

a second register to communicate information from the second core to the first core, wherein the second register includes a plurality of bits used to synchronize operation of the first core and the second core.

59. A microprocessor as recited in claim 58, wherein the first register is to communicate information only from the first core to the second core, and the second register is to communicate information only from the second core to the first core.

60. A microprocessor as recited in claim 59, wherein the first register and the second register are cross-decoded by the first core and the second core.

61. A microprocessor as recited in claim 60, wherein:

the first core is configured to execute a predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the first register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding; and

the second core is configured to execute the predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the second register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the first register is set to a predetermined value before proceeding.

62. An apparatus comprising:

a first register to communicate information from a first processing entity of a microprocessor to a second processing entity of the microprocessor;

a second register to communicate information from the second processing entity to the first processing entity;

means for cross-decoding the first register and the second register between the first processing entity and the second processing entity.

means for causing the first processing entity to set a predetermined bit of a plurality of bits in the first register to a predetermined value;

means for causing the first processing entity to wait until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding.

63. An apparatus as recited in claim 62, wherein the first and second processing entities are separate cores of the microprocessor.

64. An apparatus as recited in claim 62, wherein the first and second processing entities are separate threads of the microprocessor.

65. A computer system comprising:

a microprocessor including

a first core;

a second core;

a first register to communicate information from the first core to the second core, wherein the first register includes a plurality of bits used to synchronize operation of the first core and the second core; and

a second register to communicate information from the second core to the first core, wherein the second register includes a plurality of bits used to synchronize operation of the first core and the second core;

and

a shared cache coupled to the first core and the second core;

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

66. A computer system as recited in claim 65, wherein the first register is to communicate information only from the first core to the second core, and the second register is to communicate information only from the second core to the first core.

67. A computer system as recited in claim 66, wherein the first register and the second register are cross-decoded by the first core and the second core.

68. A computer system as recited in claim 67, wherein:

the first core is configured to execute a predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the first register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding; and

the second core is configured to execute the predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the second register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the first register is set to a predetermined value before proceeding.